WHAT IS CLAIMED IS:

1. A method comprising:

in response to a data read request for requested data:

allocating an area of memory to the requested data, the memory area being divided into at least one memory chunk;

writing a seed value to one or more of the at least one memory chunk; and

in response to completion of at least one write transaction corresponding to the data read request, for each of the one or more memory chunks having a seed value, validating the integrity of each of the at least one write transaction based, at least in part, on the seed value.

2. The method of claim 1, wherein said validating the integrity of a given one of the at least one write transaction comprises, for a given memory chunk:

determining if the memory chunk includes the seed value; and

if the memory chunk includes the seed value, determining that the given write transaction is invalid.

3. The method of claim 2, wherein said determining if the memory chunk includes the seed value comprises determining if the memory chunk includes the seed value at specified bits of the memory chunk.

4. The method of claim 2, additionally comprising modifying the seed value if the write transaction is determined to be invalid.

5. The method of claim 1, wherein the size of the seed value is based on a specified error rate of the device.

6. An apparatus comprising:

circuitry capable of responding to a data read request for requested data by:

allocating an area of memory to the requested data, the memory area being divided into at least one memory chunk;

writing a seed value to one or more of the at least one memory chunk; and

responding to completion of at least one write transaction corresponding to the data read request by, for each of the one or more memory chunks having a seed value, validating the integrity of each of the at least one write transaction based, at least in part, on the seed value.

7. The apparatus of claim 6, wherein said circuitry capable of validating the integrity of a given one of the at least one write transaction is capable of, for a given memory chunk:

determining if the memory chunk includes the seed value; and

if the memory chunk includes the seed value, determining that the given write transaction is invalid.

8. The apparatus of claim 7, wherein said circuitry capable of determining if the memory chunk includes the seed value is capable of determining if the memory chunk includes the seed value at specified bits of the memory chunk.

9. The apparatus of claim 7, wherein said circuitry is additionally capable of modifying the seed value if the write transaction is determined to be invalid.

10. The apparatus of claim 6, wherein the size of the seed value is based on a specified error rate of the device.

11. A system comprising:

a PCI-E (Peripheral Component Interconnect - Enhanced) bus;

a buffer communicatively coupled to the PCI-E bus, the buffer being divided into at least one memory chunk; and

circuitry capable of responding to a data read request for requested data by:

allocating the buffer to the requested data, the buffer being divided into at least one memory chunk;

writing a seed value to one or more of the at least one memory

chunk; and

responding to completion of at least one write transaction corresponding to the data read request by, for each of the one or more memory chunks having a seed value, validating the integrity of each of the at least one write transaction based, at least in part, on the seed value.

12. The system of claim 11, wherein said circuitry capable of validating the integrity of a given one of the at least one write transaction is capable of, for a given memory chunk:

determining if the memory chunk includes the seed value; and

if the memory chunk includes the seed value, determining that the given write transaction is invalid.

13. The system of claim 12, wherein said circuitry capable of determining if the memory chunk includes the seed value is capable of determining if the memory chunk includes the seed value at specified bits of the memory chunk.

14. The system of claim 12, wherein said circuitry is additionally capable of modifying the seed value if the write transaction is determined to be invalid.

15. The system of claim 11, wherein the size of the seed value is based on a specified error rate of the device.

16. An article comprising a machine-readable medium having machine-accessible instructions, the instructions when executed by a machine, result in the following:

responding to a data read request for requested data by:

allocating an area of memory to the requested data, the memory area being divided into at least one memory chunk;

writing a seed value to one or more of the at least one memory chunk; and

responding to completion of at least one write transaction corresponding to the data read request by, for each of the one or more memory chunks having a seed value, validating the integrity of each of the at least one write transaction based, at least in part, on the seed value.

17. The article of claim 16, wherein said instructions that result in validating the integrity of a given one of the at least one write transaction comprise instructions that result in, for a given memory chunk:

determining if the memory chunk includes the seed value; and

if the memory chunk includes the seed value, determining that the given write transaction is invalid.

18. The article of claim 17, wherein the instructions that result in determining if

the memory chunk includes the seed value comprise instructions that result in determining if the memory chunk includes the seed value at specified bits of the memory chunk.

19. The article of claim 17, additionally comprising instructions that result in modifying the seed value if the write transaction is determined to be invalid.

20. The article of claim 16, wherein the size of the seed value is based on a specified error rate of the device.